ACS APPLIED MATERIALS & INTERFACES

Research Article

www.acsami.org

Tailoring the Interface Quality between HfO_2 and GaAs via *in Situ* ZnO Passivation Using Atomic Layer Deposition

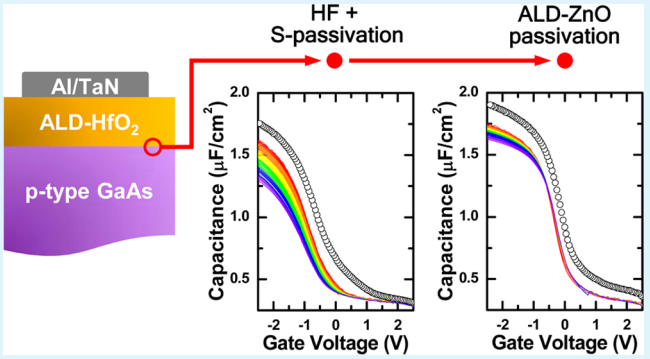
Young-Chul Byun,[†,§] Sungho Choi,[†] Youngseo An,[†] Paul C. McIntyre,[‡] and Hyoungsub Kim*[,†]

[†]School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon 440-746, Korea

[‡]Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, United States

Supporting Information

ABSTRACT: We investigated ZnO surface passivation of a GaAs (100) substrate using an atomic layer deposition (ALD) process to prepare an ultrathin ZnO layer prior to ALD–HfO_2 gate dielectric deposition. Significant suppression of both Ga–O bond formation near the interface and As segregation at the interface was achieved. In addition, this method effectively suppressed the trapping of carriers in oxide defects with energies near the valence band edge of GaAs. According to electrical analyses of the interface state response on p- and n-type GaAs substrates, the interface states in the bottom half of the GaAs band gap were largely removed. However, the interface trap response in the top half of the band gap increased somewhat for the ZnO-passivated surface.



KEYWORDS: *ZnO, GaAs, atomic layer deposition, surface passivation, electrical property*

1. INTRODUCTION

Because of the mobility limitations in conventional Si channels, III–V channel materials such as GaAs, InGaAs, and InP are being developed to further boost the performance of metal oxide semiconductor field effect transistors (MOSFETs) in the near future. Accordingly, extensive research has been conducted for more than a decade and has focused specifically on minimizing the number of near-interface defects (interface states and border traps) between the high-*k* gate dielectric and the III–V channel layer.[1,2]

In an effort to improve the interface quality, several wet cleaning techniques have been adopted using $(NH_4)_2S$ and NH_4OH.[3−5] Moreover, additional interface passivation layers (IPLs), such as Si,[6] Ge,[7] Ga_2O_3 (Gd_2O_3),[8] AlN,[9] TaON,[10] and Al_2O_3,[11] have been suggested. As an alternative approach, Kundu et al. recently reported an improvement in the interface characteristics by introducing a ZnO IPL (~2 nm) grown by a metal–organic chemical vapor deposition technique on p-type GaAs substrates, which was followed by the deposition of sol–gel-processed TiO_2 and ZrO_2 gate dielectrics.[12−14] However, the deposition method for both the high-*k* dielectric and IPL may not be acceptable for state-of-the-art device fabrication. Furthermore, the *ex situ* deposition process may engender unintended extra contamination at the interface between the high-*k* dielectric and IPL. Chen et al.[15] more recently obtained a similar improvement in the interface quality by adopting an atomic layer deposition (ALD) method for both the Al_2O_3 film and ZnO IPL (~2 nm) on n-type GaAs. ALD is a state-of-the-art technique for gate dielectric formation because it achieves excellent film thickness control, pinhole-free films with small thicknesses, and conformal deposition around complex nanoscale features.[16] An advantage of using ALD as a surface passivation method prior to gate dielectric deposition is that it allows an *in situ* process without a vacuum break, which may be beneficial in further improving the interface quality.

In this paper, we used an ALD method in forming both the high-*k* HfO_2 film and ZnO IPL on GaAs, and we intensively investigated the effect of ALD–ZnO passivation on the electrical properties when different doping types of GaAs substrates were used (p- and n-type) to probe the energy distribution of charge trapping defects across the GaAs band gap. For the formation of an ultrathin ZnO IPL, only 10 cycles of the ALD–ZnO process were conducted at 150 °C, which is not enough to form a complete layer because of the extensive incubation regime of this process.[17] Therefore, the ALD–ZnO process prior to HfO_2 formation may result in a surface treatment rather than the formation of a physically distinct ZnO IPL.

2. EXPERIMENTAL SECTION

Both (100)-oriented p-type (Zn-doped, 5.6–5.9 × 10^{17} cm^{-3}) and n-type (Si-doped, 8–40 × 10^{17} cm^{-3}) GaAs were used as substrates. The substrates were cleaned by being dipped in an ~1% HF solution and passivated with sulfur (S) using an ~21% $(NH_4)_2S$ solution, which is known to be effective for the removal of Ga/As-related oxides and corresponding interface defects.[18] As a reference sample, as-received

Received: April 4, 2014
Accepted: June 9, 2014
Published: June 9, 2014

GaAs substrates without any cleaning were also used for HfO_2 deposition. The as-received and S-passivated GaAs substrates were immediately loaded into an ALD vacuum chamber within 3 min to minimize ambient contamination. HfO_2 films were deposited at 200 °C using tetrakis(ethylmethylamino)hafnium (TEMAHf) and H_2O precursors in a laboratory-scale thermal ALD system by injecting the TEMAHf first. The number of ALD cycles was fixed at 110, which is expected to form an HfO_2 film with a thickness of ~8 nm. The HfO_2 film thickness was confirmed by both ellipsometry and high-resolution transmission electron microscopy (HRTEM, JEOL JEM ARM 200F). For the preparation of the ZnO-passivated samples, some of the S-passivated GaAs substrates were additionally treated with an ALD−ZnO process utilizing diethylzinc (DEZ) and H_2O precursors for 10 cycles at 150 °C. In the same way that was used in the ALD−HfO_2 process, a metal−organic precursor (DEZ) was introduced first instead of the oxidant. After the ALD−ZnO process, the sample temperature was increased to 200 °C over 5 min to deposit the HfO_2 film *in situ*.

For the identification of the near-interface chemical bonding configuration with different starting surface conditions, some samples were deposited at an HfO_2 thickness of ~2.5 nm and characterized by X-ray photoelectron spectroscopy [XPS, AXIS-NOVA (Kratos Inc.) located at the Korea Basic Science Institute, Jeonju, Korea] equipped with a monochromatic Al Kα (1486.7 eV) X-ray source. To investigate the out-diffusion behavior of substrate elements (Ga and As), as-deposited, ~8 nm thick HfO_2 films on n-type GaAs substrates with different surface conditions were measured by time-of-flight secondary ion mass spectroscopy (ToF-SIMS, ION-TOF TOF.SIMS-5). For the depth profiling of Ga and As atoms, Cs^+ and O_2^+ sputtering guns with a Bi^+ analysis gun were used, respectively, in a dual-beam mode.

The electrical properties of the prepared samples were evaluated by fabricating MOS capacitors with sputter-deposited Al (10 nm)/TaN (50 nm) gate electrodes (area of 7850 μm^2) patterned by a lift-off process. All the capacitor samples underwent forming gas (4% H_2 in N_2) annealing at 400 °C for 30 min after the metallization step. Capacitance−voltage (C−V) and conductance−voltage (G−V) characteristics were assessed at different ac frequencies varying logarithmically from 100 Hz to 1 MHz as a function of gate voltage in a parallel mode using an Agilent E4980A LCR meter and a B1500A semiconductor device analyzer. During the measurement, the gate voltage was scanned in a direction from inversion to accumulation. The leakage current was measured using a Keithley 6514 electrometer while applying a gate bias using a Keithley 230 programmable voltage source.

3. RESULTS AND DISCUSSION

The effect of ALD−ZnO passivation on the change in interfacial chemical bonding between HfO_2 and the GaAs substrate was examined by collecting Ga 2p and As 3d XPS spectra, as shown in Figures 1 and 2, respectively. The measured binding energy scale of the spectra was referenced to a reported As $3d_{5/2}$ peak of 40.8 eV, coming from the substrate (As−Ga) to compensate for possible charging.[19] In addition, peak fitting was conducted on the basis of the chemical shifts described in ref 19. Panels a−c of Figure 1 show the Ga $2p_{3/2}$ spectra overlapped with three fitted subpeaks: Ga−As (in GaAs), Ga^+ (in Ga_2O), and Ga^{3+} (in Ga_2O_3). Although some degree of self-cleaning by exposure to the TEMAHf precursor might occur to reduce the amount of native oxide,[20] substantial Ga−O bonding was detected in the HfO_2−GaAs interface region of the sample prepared on the as-received GaAs surface. After native oxide removal and S passivation via aqueous HF and $(NH_4)_2S$ cleaning, Ga^+ and Ga^{3+} peak intensities were significantly reduced compared to those in the sample without any *ex situ* cleaning. When an additional treatment using the ALD−ZnO process was adopted following S passivation, a further decrease in Ga^+ peak intensity was observed compared with the substrate peak intensity (see Figure 1d). Because the S passivation process can form Ga−S bonds, which have a binding energy similar to that of the Ga^+ state,[21] it is also possible that desorption of S during the subsequent ALD−ZnO process at 150 °C contributes to the decrease in the Ga^+ peak intensity.

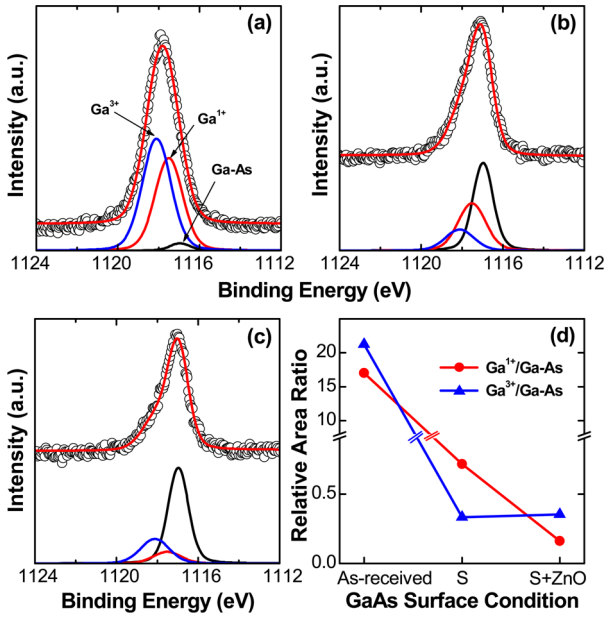


Figure 1. Ga $2p_{3/2}$ XPS spectra obtained from ALD−HfO_2 films on n-type GaAs with different surface conditions: (a) as received, (b) HF and $(NH_4)_2S$-cleaned, and (c) GaAs surfaces subjected to additional ALD−ZnO passivation. (d) Relative area ratios of deconvoluted Ga^+ and Ga^{3+} peaks with respect to that of the Ga−As peak.

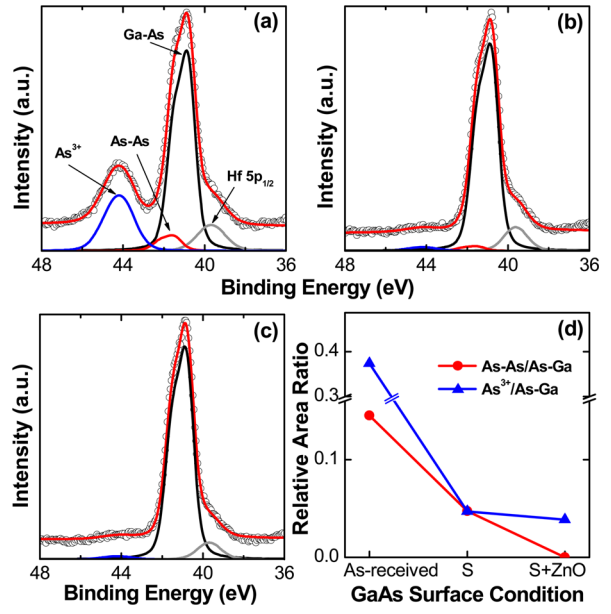


Figure 2. As 3d XPS spectra obtained from ALD−HfO_2 films on n-type GaAs with different surface conditions: (a) as received, (b) HF and $(NH_4)_2S$-cleaned, and (c) GaAs surfaces subjected to additional ALD−ZnO passivation. (d) Relative area ratios of deconvoluted elemental As and As^{3+} peaks with respect to that of the Ga−As peak.

In the case of the As 3d spectra shown in Figure 2, four distinctive subpeaks were identified: As−Ga (in GaAs), As−As (elemental As), As^{3+} (in As_2O_3), and Hf $5p_{1/2}$ (in HfO_2). Even for the HfO_2 sample prepared on the as-received GaAs surface,

no measurable As^{5+} (in As_2O_5) peak was identified, which is consistent with the reported self-cleaning effect by the TEMAHf precursor during the ALD process.[20] After S passivation (Figure 2b), large decreases in As^{3+} and As−As peak intensities were observed, as reported in a previous study.[18] In comparison with the Ga 2p case, it is difficult to detect a notable reduction of As-related subpeaks after ALD−ZnO treatment, as shown in panels c and d of Figure 2; this may be due to the lower sensitivity of XPS for As oxides compared to that of the Ga−As substrate feature in the As 3d spectral region. The chemical bonding status of Zn atoms was also monitored by XPS, as shown in Figure 3. The binding energy of the Zn $2p_{3/2}$ peak was ∼1021.8 eV, which is believed to correspond to Zn−O bonding.

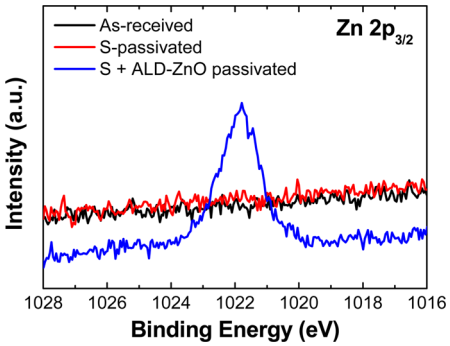


Figure 3. Zn $2p_{3/2}$ XPS spectra collected from the ALD−HfO_2 films deposited on n-type GaAs substrates under different surface conditions.

Depth profiles of substrate elements, i.e., Ga and As, were measured using ToF-SIMS, as shown in Figure 4. For the $^{75}As^-$ profile (Figure 4a−c), a significant segregation of As atoms at the HfO_2 and GaAs interface (highlighted by a red, dashed circle) was observed in the sample prepared on the as-received GaAs. When the native oxide was removed and the substrate was treated with HF and $(NH_4)_2S$, the extent of As segregation was reduced; further reduction was achieved by additional ALD−ZnO treatment. In contrast to the As^- case, the $^{69}Ga^+$ profiles shown in panels d−f of Figure 4 suggested a modest diffusion of Ga atoms into the HfO_2 film even during the ALD process, as observed in other studies.[22,23] It is known that a GaAs surface that has undergone intentional or unintentional (such as the ALD high-*k* process) oxidation strongly prefers formation of Ga oxides over As oxides and produces an As-rich surface.[24] Therefore, the diffused Ga atoms are thought to be bonded to oxygen in the HfO_2 film (detected as Ga−O bonds by XPS measurement), while As atoms segregate in the interface. Via combination of the XPS and ToF-SIMS results, we can conclude that the ALD−ZnO treatment is more effective than the investigated S passivation process in suppressing Ga diffusion (Ga−O bond formation) near the interface region and local As segregation at the interface.

As a representative electrical measurement of interface quality, single-sweep, multifrequency *C*−*V* characteristics are compared first on p-type GaAs samples, as shown in Figure 5. To obtain the best representation of interface trap responses across most of the GaAs band gap (∼1.4 eV), high-temperature (150 °C) measurements were performed together with room-temperature measurements. Quasi-static *C*−*V* (QSCV) curves were also obtained to monitor the maximal accumulation capacitance (C_{max}) and the overall amount of interface states. In addition, as a reference, the ideal oxide capacitance (C_{ox}) was calculated for each sample and is included in Figure 5 for comparison. For this calculation, the physical thicknesses of the ALD−HfO_2 films were measured by a separate HRTEM analysis [as received, ∼8.5 nm; S-passivated, ∼8.2 nm; ZnO-passivated, ∼8.0 nm (see Figure S1 of the Supporting Information)], and the dielectric constant of the ALD−HfO_2 film was estimated to be ∼17 by the thickness series samples on the HF-cleaned Si substrate.

In the negative bias range where accumulation appears to be occurring, there is huge frequency dispersion in the as-received sample (panels a and d of Figure 5). The frequency dispersion is somewhat suppressed after the native oxide removal and S passivation processes and greatly suppressed after the additional ALD−ZnO passivation. The dispersive character in the accumulation region is mainly attributed to a high density of border traps[2,25] located close to (<1−1.5 nm from) the

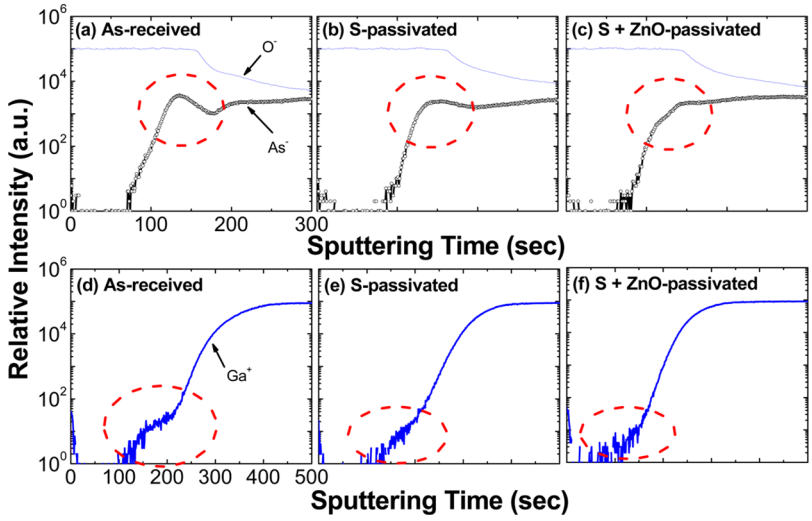


Figure 4. ToF-SIMS depth profiles of ∼8 nm HfO_2 on n-type GaAs samples: (a−c) $^{75}As^-$ profile and (d−f) $^{69}Ga^+$ profile. The GaAs substrates were subjected to different surface conditions: (a and d) as received, (b and e) HF and $(NH_4)_2S$-cleaned, and (c and f) GaAs surfaces subjected to additional ALD−ZnO passivation.

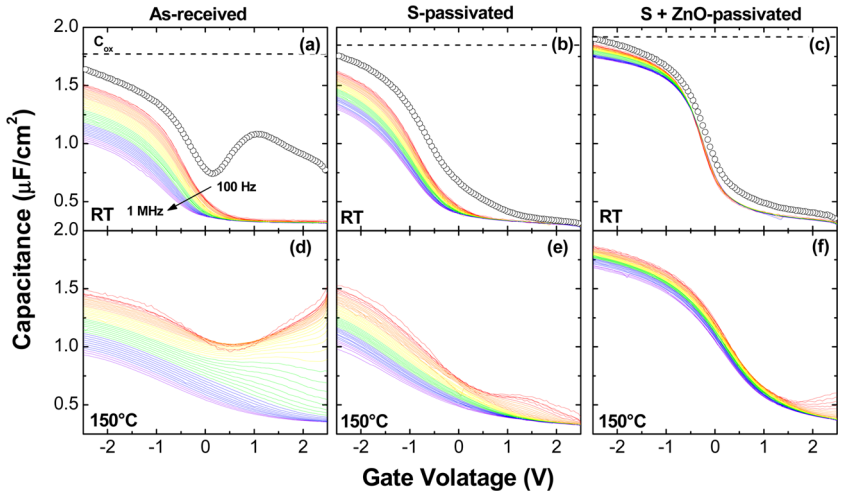


Figure 5. Multifrequency $C-V$ characteristics of HfO_2 on p-type GaAs capacitors measured at (a–c) room temperature and (d–f) 150 °C. The p-type GaAs substrates were subjected to different surface conditions: (a and d) as received, (b and e) HF and $(NH_4)_2S$-cleaned, and (c and f) surfaces subjected to additional ALD–ZnO passivation. The solid lines show high-frequency $C-V$ curves measured from 100 Hz to 1 MHz, and the symbols show the QSCV characteristics.

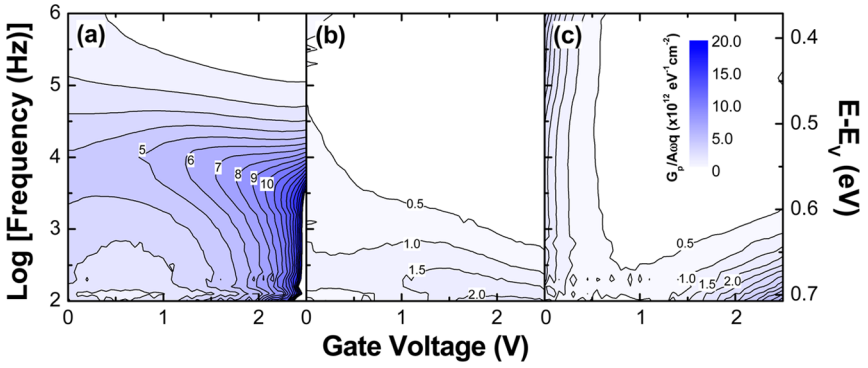


Figure 6. $G_p/A\omega q$ contour maps of HfO_2 on p-type GaAs capacitors with different GaAs surface conditions: (a) as received, (b) HF and $(NH_4)_2S$-cleaned, and (c) surfaces subjected to additional ALD–ZnO passivation. The measurements were recorded at 150 °C. The right y-axis is the energy level with respect to the valence band edge (E_V) of GaAs corresponding to the measurement frequency.

interface with energy levels near the band edge of the majority carrier band. Therefore, this suggests that the as-received GaAs sample, which has the most defective interlayer from the XPS data, exhibits the greatest border trap density located near the valence band (VB) edge of p-type GaAs. Accordingly, S and ALD–ZnO passivation may produce a more abrupt HfO_2–GaAs interface by removing most of the residual native oxides (especially Ga oxide) and metallic As.

In the case of the bias range associated with the depletion and inversion regions, the increase in the measurement temperature incurred an additional appearance of frequency dispersion in the samples formed on the as-received p-type GaAs substrate (Figure 5d). Because an increase in measurement temperature can trigger the response of the interface states located closer to the midgap region,[26] the appearance of the frequency-dependent increase in the inversion capacitance implies that the substrate is unable to enter depletion for the as-received p-GaAs case. In the case of the QSCV characteristics, GaAs is known to produce no increase in inversion capacitance because of its extremely low intrinsic carrier concentration (n_i) of ~10^6 cm^{-3} at room temperature.[27] However, a peak-shaped, large increase in the inversion capacitance was observed in the sample prepared on the as-received GaAs, which can be mostly ascribed to the presence of a trap-induced capacitance. This further confirms the existence of a large number of interface states near the VB edge. Similar to the trend in the accumulation region, S passivation greatly alleviated the frequency-dependent increase in the inversion capacitance and much more suppression was achieved via ALD–ZnO passivation.

To more clearly understand the ac response of the interface states located in the bottom of the GaAs band gap, parallel conductance (G_p) was measured at 150 °C with respect to measurement frequency (f) and voltage on the p-type GaAs samples. The contour maps of normalized parallel conductance ($G_p/A\omega q$) are drawn for three p-type samples in Figure 6, where A is the capacitor area, ω is the angular frequency ($2\pi f$), and q is elementary charge.[28] The approximate range of energies in the GaAs band gap with respect to the VB edge (E_V) that are probed by varying the measurement frequency is expressed on the right y-axis in Figure 6 using the following equation:[28,29]

$$E - E_V = kT \ln\left(\frac{\upsilon_{th}\sigma N}{\omega}\right)$$

where k is Boltzmann's constant and T is the measurement temperature. An average hole thermal velocity (υ_{th}) of 1.8×10^7 cm s^{-1}, a capture cross section (σ) of 1×10^{-15} cm^2, and a

dx.doi.org/10.1021/am502048d | ACS Appl. Mater. Interfaces 2014, 6, 10482–10488

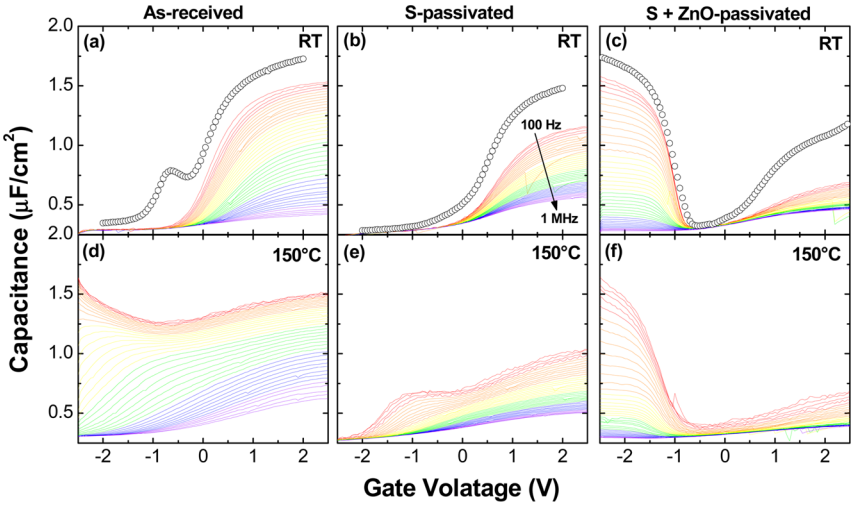


Figure 7. Multifrequency $C-V$ characteristics of HfO_2 on n-type GaAs capacitors measured at (a–c) room temperature and (d–f) 150 °C. The n-type GaAs substrates were subjected to different surface conditions: (a and d) as received, (b and e) HF and $(NH_4)_2S$-cleaned, and (c and f) surfaces subjected to additional ALD–ZnO passivation. The solid lines show the high-frequency $C-V$ curves measured from 100 Hz to 1 MHz, and the symbols show the QSCV characteristics.

density of states (N) of 9.0×10^{18} cm^{-3} in the VB were assumed.[29] Coinciding with the multifrequency $C-V$ responses, the Fermi level is strongly pinned near the VB edge of GaAs for the as-received sample. In contrast, the Fermi level pinning is somewhat relieved by S passivation, and a nearly complete depinning from the VB edge is allowed by the additional ZnO passivation. In the case of the high k on GaAs, As dangling bonds are predicted to produce most of the interface states that tail in from the VB edge into the GaAs band gap.[24] This suggests that the ALD–ZnO passivation process is effective in reducing the number of As dangling bonds. One thing to be noted here is a false inversion response observed at a more positive gate bias in the ZnO-passivated sample (Figure 5f), which indicates the presence of a significant defect density in the top half of the GaAs band gap, probably Ga dangling bonds and As–Ga antisites.[24]

Frequency-dependent $C-V$ and QSCV characteristics were also examined on n-type GaAs substrates with different starting surfaces, as shown in Figure 7. When the response of the interface states is largely activated (150 °C measurement), the $C-V$ curves of the as-received n-type GaAs sample show evidence of Fermi level pinning in inversion for all gate biases, as shown in Figure 7d. This inversion behavior is suppressed at the most negative gate biases after the introduction of S passivation, as shown in Figure 7e. This is likely because the interface state density in the bottom half of the GaAs band is revealed to be somewhat smaller for the S-passivated GaAs than for the as-received GaAs, according to the aforementioned analysis performed on the p-type GaAs samples. A key point for both samples is that they cannot be easily depleted once they exhibit surface inversion. Furthermore, they never properly accumulate, which makes it difficult to differentiate the degree of border trap response in the accumulation region.

When the ALD–ZnO treatment was performed on the S-passivated n-type GaAs substrate, the inversion behavior was dramatically changed; that is, little change in capacitance versus gate voltage for a given ac frequency is observed. The inversion capacitance of the QSCV curve nearly reaches the ideal C_{ox} value, which is unexpected given the low density of states in the conduction band of GaAs. One possible reason for this phenomenon is peripheral inversion observed in a couple of high-k MOS capacitors.[30] The MOS capacitor is not inverted under the gate at zero bias, but it does invert at more negative biases by extending an inversion layer in the n-type GaAs periphery under the gate. Because the peripheral inversion is strongly dependent on the MOS capacitor size, additional multifrequency $C-V$ measurements were performed on the ZnO-passivated samples with different pattern sizes. As revealed in Figure S2 of the Supporting Information, the larger capacitors exhibited a suppressed dispersion behavior in the inversion region. Although the capacitor size dependency is somewhat small compared to the reported experimental result,[30] it can be assumed that the observed inversion dispersion on the ZnO-passivated sample is partly attributed to the peripheral inversion behavior. Another possible reason for this anomalous inversion behavior could be doping during the ALD–ZnO process performed on the n-type GaAs substrate. Because Zn can act as a p-type dopant in GaAs,[31] it can create acceptor energy levels in the n-type GaAs band gap and, thereby, may induce a strong minority carrier response.

When the gate voltage approaches the depletion region, the lack of an apparent false inversion response at zero bias indicates that the ZnO-passivated n-type GaAs sample can be depleted, similar to the sample on the p-type GaAs (see Figure 5f). This is consistent with an As dangling bond density lower than those for the other two n-type GaAs samples, once again providing a consistent picture compared to the p-type GaAs data. However, the ZnO-passivated sample does not accumulate properly, as shown in panels c and f of Figure 7, which indicates that the Fermi level is pinned in the top half of the GaAs band gap. In comparison with the as-received and S-passivated samples, the ZnO-passivated sample exhibits a much smaller accumulation capacitance for both room- and high-temperature measurements. Although a clear identification of the possible origin is not available, it is presumed that a large number of additional interface states are newly created near the conduction band (CB) edge of GaAs by the ZnO passivation, the origin of which is being studied.

In terms of the hysteresis characteristics during the bidirectional sweep of $C-V$ curves, a significant reduction in

the level of hysteresis was obtained on the ALD−ZnO-passivated p-type GaAs sample as compared with the as-received and S-passivated samples (Figure 8a): ∼480 mV for

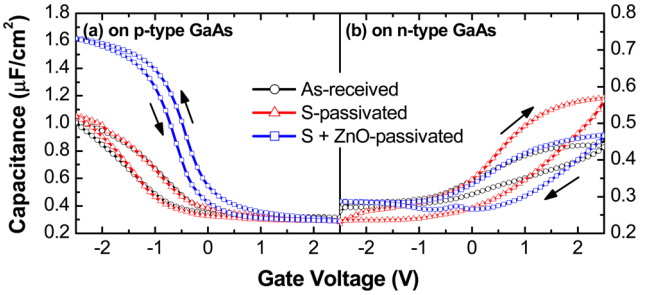


Figure 8. Bidirectional 1 MHz $C-V$ characteristics of ALD−HfO_2 films on (a) p-type and (b) n-type GaAs substrates under different surface conditions.

the as-received and S-passivated samples and ∼270 mV for the ZnO-passivated sample. However, on the n-type substrates, an increase in the level of hysteresis was observed for the ZnO-passivated sample compared to those of other samples (Figure 8b): ∼1100 mV for the as-received and S-passivated samples and ∼1250 mV for the ZnO-passivated sample.

Lastly, the leakage current characteristics with different surface passivation conditions were evaluated on both p- and n-type GaAs substrates, as shown in Figure 9. The gate voltage

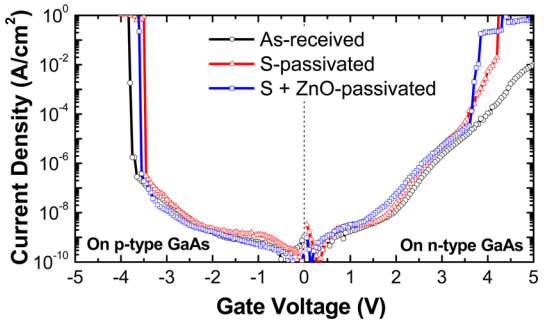


Figure 9. Leakage current characteristics of the HfO_2 films measured on p- and n-type GaAs substrates under different surface conditions.

was varied in a negative (electron injection from the gate electrode) and a positive (electron injection from GaAs substrate) direction on the p- and n-type GaAs cases, respectively. As mentioned above, the HfO_2 thickness on the ZnO-passivated GaAs surface was slightly smaller than that on other GaAs surfaces (see HRTEM images in Figure S1 of the Supporting Information). Nevertheless, no detrimental increase in the leakage current was identified even after the introduction of ALD−ZnO passivation on the GaAs substrates.

4. CONCLUSION

Prior to the formation of ALD−HfO_2 films, ALD−ZnO treatment for 10 cycles was investigated on GaAs substrates, and their electrical properties were compared with those of as-received and S-passivated GaAs with different doping types. ALD−ZnO passivation greatly reduced the extents of diffusion-mediated Ga−O bond formation and near-interface As segregation. According to the $C-V$ analysis of both p- and n-type substrates, many border traps in the HfO_2 film aligned near the VB edge of GaAs were effectively removed. In terms of the interface states, the ALD−ZnO process effectively passivated interface traps in the bottom half of the GaAs band gap, which resulted in a significant improvement in $C-V$ characteristics on p-type GaAs substrates. However, it still left a high density of defects in the top half of the band gap, which were also, apparently, not fully addressed by the S treatment. In addition, as an adverse effect, $C-V$ characteristics on n-type GaAs were degraded even more because of the additional ALD−ZnO passivation. With regard to the leakage current characteristics, there was no harmful effect caused by the introduction of an ALD−ZnO passivation process. Although the ALD−ZnO passivation is not a preferable technique on the n-type GaAs, it is expected that its application on the p-type GaAs for an inversion-mode MOSFET is quite promising.

■ ASSOCIATED CONTENT

Supporting Information

Cross-sectional HRTEM images and capacitor area-dependent $C-V$ curves measured from the ALD−HfO_2 films deposited on GaAs substrates under different surface conditions. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: hsubkim@skku.edu.

Present Address

§Y.-C.B.: Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by the Future Semiconductor Device Technology Development Program (Grant 10045216) funded by MOTIE (Ministry of Trade, Industry & Energy) and KSRC (Korea Semiconductor Research Consortium). We thank Prof. Weichao Wang (Nankai University, Tianjin, China) and Prof. Kyeongjae Cho (The University of Texas at Dallas, Richardson, TX) for helpful discussions.

■ REFERENCES

(1) Hurley, P. K.; O'Connor, É.; Djara, V.; Monaghan, S.; Povey, I. M.; Long, R. D.; Sheehan, B.; Lin, J.; McIntyre, P. C.; Brennan, B.; Wallace, R. M.; Pemble, M. E.; Cherkaoui, L. The Characterization and Passivation of Fixed Oxide Charges and Interface States in the Al_2O_3/InGaAs MOS System. *IEEE Trans. Device Mater. Reliab.* **2013**, *13*, 429−443.

(2) Simoen, E.; Lin, D. H.; Alian, A.; Brammertz, G.; Merckling, C.; Mitard, J.; Claeys, C. Border Traps in Ge/III-V Channel Devices: Analysis and Reliability Aspects. *IEEE Trans. Device Mater. Reliab.* **2013**, *13*, 444−455.

(3) Shahrjerdi, D.; Tutuc, E.; Banerjee, S. K. Impact of Surface Chemical Treatment on Capacitance-Voltage Characteristics of GaAs Metal-Oxide-Semiconductor Capacitors with Al_2O_3 Gate Dielectric. *Appl. Phys. Lett.* **2007**, *91*, 063501.

(4) Byungha, S.; Choi, D.; Harris, J. S.; McIntyre, P. C. Pre-Atomic Layer Deposition Surface Cleaning and Chemical Passivation of (100) $In_{0.2}Ga_{0.8}As$ and Deposition of Ultrathin Al_2O_3 Gate Insulators. *Appl. Phys. Lett.* **2008**, *93*, 052911.

(5) Aguirre-Tostado, F. S.; Milojevic, M.; Choi, K. J.; Kim, H. C.; Hinkle, C. L.; Vogel, E. M.; Kim, J.; Yang, T.; Xuan, Y.; Ye, P. D.; Wallace, R. M. S passivation of GaAs and Band Bending Reduction

upon Atomic Layer Deposition of HfO_2/Al_2O_3 Nanolaminates. *Appl. Phys. Lett.* **2008**, *93*, 061907.
(6) Koveshnikov, S.; Tsai, W.; Ok, I.; Lee, J. C.; Torkanov, V.; Yakimov, M.; Oktyabrsky, S. Metal-Oxide-Semiconductor Capacitors on GaAs with High-k Gate Oxide and Amorphous Silicon Interface Passivation Layer. *Appl. Phys. Lett.* **2006**, *88*, 022106.
(7) Kim, H.-S.; Ok, I.; Zhang, M.; Lee, T.; Zhu, F.; Yu, L.; Lee, J. C.; Koveshnikov, S.; Tsai, W.; Tokranov, V.; Yakimov, M.; Oktyabrsky, S. Depletion-Mode GaAs Metal-Oxide-Semiconductor Field-Effect Transistor with HfO_2 Dielectric and Germanium Interfacial Passivation Layer. *Appl. Phys. Lett.* **2006**, *89*, 222904.
(8) Passlack, M.; Hong, H.; Mannaerts, J. P. Quasistatic and High Frequency Capacitance−Voltage Characterization of Ga_2O_3−GaAs Structures Fabricated by In Situ Molecular Beam Epitaxy. *Appl. Phys. Lett.* **1996**, *8*, 1099−1101.
(9) Jussila, H.; Mattila, P.; Oksanen, J.; Perros, A.; Riikonen, J.; Bosund, M.; Varpula, A.; Huhtio, T.; Lipsanen, H.; Sopanen, M. High-k GaAs Metal Insulator Semiconductor Capacitors Passivated by Ex-Situ Plasma-Enhanced Atomic Layer Deposited AlN for Fermi-Level Unpinning. *Appl. Phys. Lett.* **2012**, *100*, 071606.
(10) Wang, L. S.; Xu, J. P.; Zhu, S. Y.; Huang, Y.; Lai, P. T. Improved Interfacial and Electrical Properties of GaAs Metal-Oxide-Semiconductor Capacitors with HfTiON as Gate Dielectric and TaON as Passivation Interlayer. *Appl. Phys. Lett.* **2013**, *103*, 092901.
(11) Kim, T.-W.; Kim, D.-H.; Koh, D. H.; Kwon, H. M.; Baek, R. H.; Veksler, D.; Huffman, C.; Matthews, K.; Oktyabrsky, S.; Greene, A.; Ohsawa, Y.; Ko, A.; Nakajima, H.; Takahashi, M.; Nishizuka, T.; Ohtake, H.; Banerjee, S. K.; Shin, S. H.; Ko, D.-H.; Kang, C.; Gilmer, D.; Hill, R. J. W.; Maszara, W.; Hobbs, C.; Kirsch, P. D. Sub-100 nm InGaAs Quantum-Well (QW) Tri-Gate MOSFETs with Al_2O_3/HfO_2 (EOT < 1 nm) for Low-Power Logic Applications. *Int. Electron Devices Meet.* **2013**, 425−428.
(12) Kundu, S.; Shripathi, T.; Banerji, P. Interface Engineering with an MOCVD Grown ZnO Interface Passivation Layer for ZrO_2−GaAs Metal−Oxide−Semiconductor Devices. *Solid State Commun.* **2011**, *151*, 1881−1884.
(13) Kundu, S.; Anitha, Y.; Chakraborty, S.; Banerji, P. Interface Studies on High-k/GaAs MOS Capacitors by Deep Level Transient Spectroscopy. *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom.* **2012**, *30*, 051206.
(14) Kundu, S.; Banerji, P. Metal-Oxide-Semiconductor Devices on GaAs with High-k Dielectric and MOCVD Grown ZnO Interface Passivation Layer. *Proceedings of 2011 International Conference on Nanoscience, Technology and Societal Implications*, Bhubaneswar, India, December 8−10; IEEE: New York, 2011; pp 1−6.
(15) Liu, C.; Zhang, Y.-M.; Zhang, Y.-M.; Lü, H.-L. Interfacial Characteristics of $Al/Al_2O_3/ZnO/n$-GaAs MOS Capacitor. *Chin. Phys. B* **2013**, *22*, 076701.
(16) Kim, H.; McIntyre, P. C. Atomic Layer Deposition of Ultrathin Metal-Oxide Films for Nano-Scale Device Applications. *J. Korean Phys. Soc.* **2006**, *48*, 5−17.
(17) Tapily, K.; Gu, D.; Baumgart, H. Growth Mechanism of ALD ZnO Films Investigated by Physical Characterization. *ECS Trans.* **2010**, *33*, 355−363.
(18) Chen, P. T.; Sun, Y.; Kim, E.; McIntyre, P. C.; Tsai, W.; Garner, M.; Pianetta, P.; Nishi, Y.; Chui, C. O. HfO_2 Gate Dielectric on $(NH_4)_2S$ Passivated (100) GaAs Grown by Atomic Layer Deposition. *J. Appl. Phys.* **2008**, *103*, 034106.
(19) Suri, R.; Lichtenwalner, D. J.; Misra, V. Interfacial Self Cleaning during Atomic Layer Deposition and Annealing of HfO_2 Films on Native (100)-GaAs Substrates. *Appl. Phys. Lett.* **2010**, *96*, 112905.
(20) Hinkle, C. L.; Sonnet, A. M.; Vogel, E. M.; McDonnell, S.; Hughes, G. J.; Milojevic, M.; Lee, B.; Aguirre-Tostado, F. S.; Choi, K. J.; Kim, H. C.; Kim, J.; Wallace, R. M. GaAs Interfacial Self-Cleaning by Atomic Layer Deposition. *Appl. Phys. Lett.* **2008**, *92*, 071901.
(21) Milojevic, M.; Aguirre-Tostado, F. S.; Hinkle, C. L.; Kim, H. C.; Vogel, E. M.; Kim, J.; Wallace, R. M. Half-Cycle Atomic Layer Deposition Reaction Studies of Al_2O_3 on $In_{0.2}Ga_{0.8}As$ (100) Surfaces. *Appl. Phys. Lett.* **2008**, *93*, 202902.
(22) Dalapati, G. K.; Tong, Y.; Loh, W.-Y.; Mun, H. K.; Cho, B. J. Electrical and Interfacial Characterization of Atomic Layer Deposited High-κ Gate Dielectrics on GaAs for Advanced CMOS Devices. *IEEE Trans. Electron Devices* **2007**, *54*, 1831−1837.
(23) Byun, Y.-C.; Mahata, C.; An, C.-H.; Oh, J.; Kim, H. Interfacial and Electrical Properties of HfO_2 Gate Dielectrics Grown on GaAs by Atomic Layer Deposition Using Different Oxidants. *J. Phys. D: Appl. Phys.* **2012**, *45*, 435305.
(24) Robertson, J. Model of Interface States at III-V Oxide Interfaces. *Appl. Phys. Lett.* **2009**, *94*, 152104.
(25) Kim, E. J.; Wang, L.; Asbeck, P. M.; Saraswat, K. C.; McIntyre, P. C. Border Traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) Gate Stacks and Their Passivation by Hydrogen Anneals. *Appl. Phys. Lett.* **2010**, *96*, 012906.
(26) Brammertz, G.; Lin, H.-C.; Martens, K.; Mercier, D.; Sioncke, S.; Delabie, A.; Wang, W. E.; Caymax, M.; Meuris, M.; Heyns, M. Capacitance-Voltage Characterization of GaAs−Al_2O_3 Interfaces. *Appl. Phys. Lett.* **2008**, *93*, 183504.
(27) Sze, S. M. *Physics of Semiconductor Devices*; Wiley: New York, 1981.
(28) Engel-Herbert, R.; Hwang, Y.; Stemmer, S. Comparison of Methods to Quantify Interface Trap Densities at Dielectric/III-V Semiconductor Interfaces. *J. Appl. Phys.* **2010**, *108*, 124101.
(29) Brammertz, G.; Martens, K.; Sioncke, S.; Delabie, A.; Caymax, M.; Meuris, M.; Heyns, M. Characteristic Trapping Lifetime and Capacitance-Voltage Measurements of GaAs Metal-Oxide-Semiconductor Structures. *Appl. Phys. Lett.* **2007**, *91*, 133510.
(30) O'Connor, É.; Cherkaoui, K.; Monaghan, S.; O'Connell, D.; Povey, I.; Casey, P.; Newcomb, S. B.; Gomeniuk, Y. Y.; Provenzano, G.; Crupi, F.; Hughes, G.; Hurley, P. K. Observation of Peripheral Charge Induced Low Frequency Capacitance Voltage Behaviour in Metal-Oxide-Semiconductor Capacitors on Si and GaAs Substrates. *J. Appl. Phys.* **2012**, *111*, 124104.
(31) Hudait, M. K.; Modak, P.; Hardikar, S.; Krupanidhi, S. B. Zn Incorporation and Band Gap Shrinkage in P-Type GaAs. *J. Appl. Phys.* **1997**, *82*, 4931−4937.